

The Ekspla's digital delay generator SY4000 is designed to create up to 8 delayed output pulse sequences precisely synchronized with the internal or external clock. Digital delay generators can provide precise delays for triggering, syncing, delaying, and gating events.

Our SY4000 digital delay generator is mainly employed for synchronization and control of different laser components: AOM drivers, Pockels cell drivers, laser diode drivers, flash lamp drivers, photodetectors, data acquisition systems, etc.

Ekspla can provide both encased and OEM versions of SY4000 digital delay generator. The encased digital delay generator version can be controlled via RS232, USB, LAN, WLAN and also contains a user-friendly configuration software as well as an internal power supply. These communication options as well as software are also available in SY4000 digital delay generator's OEM version and can be reached by adding additional Ekspla's OEM communication board upon customer's request. The encased digital delay generator is an optimal solution for laboratory use while SY4000 OEM version is ideal for integration and is frequently paired with an additional Ekspla's OEM communication board.





SY4000 desktop version

FEATURES

- 8 independent output channels
- ▶ Ultra-stable internal clock 0.2 ppm
- Precise delay/pulse width control in range 2 ns to 150 ms
- > 25 ps timing resolution
- Hi-accuracy synchronization (locking) to external pulse train
- ▶ Jitter < 30ps
- DAC/AWG output
- Both 50 Ω (6 outs) and differential (8 outs) outputs present
- Frequency divider / Burst (software and hardware triggered) / Gating / Single shot
- Communications:
 - OEM version CAN BUS
 - Encased version LAN, WIFI
 - (optional), RS232, USB (VCP) via REST API or DLL's.

APPLICATIONS

- Mode locked and Q-switched fs, ps & ns lasers
- Triggering of a data acquisition system
- General purpose pulse generator
- Precise system clock source
- Laser pulse train conversion into a clean clock source
- All functions above at once



SPECIFICATIONS

| Model | SY4000 | | |
|---|---|--|--|
| OUTPUT SPECIFICATIONS (GENERAL) | | | |
| Channel modes | Single shot, burst, normal, duty cycle, frequency divider | | |
| Delay range | 0 to 150 ms | | |
| Negative delay | -150 ms | | |
| Pulsewidth | 2 ns to 150 ms | | |
| Resolution | 25 ps | | |
| Accuracy | 25 ps + 0.000001 × delay | | |
| Time base | 100 MHz, 0.2 ppm | | |
| Jitter | < 30 ps | | |
| Burst mode | 1 to 65535 | | |
| Output level | 2.5 V, 4 V | | |
| Impedance | 50 Ω | | |
| Slew rate | 1.5 V/ns | | |
| OUTPUT SPECIFICATIONS (INTERNAL GE | NERATOR) | | |
| Mode | Duty cycle | | |
| Rate | 50 ns to 100 sec | | |
| Resolution | 10 ns or 300 ps | | |
| Accuracy | 5 ns + 0.000001 × period | | |
| Jitter | 100 ps RMS | | |
| Burst | 0 65535 | | |
| INPUT SPECIFICATION (EXTERNAL TRIGG | ier) | | |
| Rate | DC to 20 MHz | | |
| Threshold | 1.3 V | | |
| Input level | LVTTL, TTL | | |
| Slope | rising | | |
| Jitter | < 100 ps RMS | | |
| Delay | < 13 ns; < 70 ns | | |
| COMMUNICATION OPTIONS | | | |
| Control interfaces (OEM board) | CAN by default. RS232, USB, LAN, WLAN with additional communication board, provided upon request | | |
| Control interfaces (encased version) | CAN, RS232, USB, LAN, WLAN | | |
| POWER REQUIREMENTS | | | |
| Power supply requirements (OEM board) | 12 V DC, 500 mA | | |
| Power supply requirements (encased version) | 90264 V, 50–60 Hz | | |
| DIMENSIONS (NOT INCLUDING CONNEC | TOR) | | |
| OEM board (L \times W \times H) | 100 × 77 × 20 mm | | |
| Encased version (L \times W \times H) | 105 × 86 × 85 mm | | |
| ACCESORIES | | | |
| CAN-USB adapter | Ekspla's CAN-USB adapter is required at evaluation stage for SY4000 OEM version board if communication via CAN interface is needed. Cable between adapter and board and beetween adapter and PC are included by default | | |
| Communication board | Ekspla's communication board which allows to control SY4000 OEM board via RS232, USB, LAN, WLAN interfaces. Can be provided upon request | | |
| Input power cables | Included by default | | |

Laser diode drivers



HIGHLIGHT FUNCTIONS OF EKSPLA'S SY4000 DIGITAL DELAY GENERATOR

- Locking to an external clock source (typically photo-diode pulse train). Triggering system is locked to the laser oscillator and trigger time is always in phase with the optical pulse.
- Trigger rate control and limiter circuit. It helps to protect laser components from damage due to exceedingly high/low triggering rates.
- Single ended and differential outputs.
- Instant switch between two configurations in delay blocks. Burst counter, gate input, frequency divider or software commands may serve as the configuration switching signal sources. Configuration switch is used to control optical pulse pickers (EO or AOM) in a highly flexible manner.
- Low jitter sync pulse output used for high-speed acquisition systems like streak camera triggering.
 Typical jitter is 3...5 ps with the respect to the optical pulse.

Control connector.

Software-controllable multiplexer may divert any of the output signals to this connector to monitor what is on other connectors without disturbing them.

- Clock output: 1:1, 1:2 frequency.
- Up to 4 pulse outputs can be combined to single signals by OR, AND, NOT logical operations.
- DAC output, controlling, e.g. AOM pass though.

INPUT/OUTPUT SIGNAL DESCRIPTION



COAXIAL CONNECTORS, A-SIDE, BNC TYPE

| Name | Description | Amplitude | Pulse parameters | Shape |
|-------------|--|--|--|---|
| PRET OUT | Precise trigger, locked to the optical clock. Delay is adjustable in optical clock period time units. Jitter in respect to the optical pulse is ~4 ps RMS, almost independent on delay | >1 V on 50 Ω, AC output, capacitor @ output | Rise time ~200 ps, width adjustable >100 ns | Positive pulse |
| TRIG1 OUT | General purpose or control sync out | 2.5 V @ 50 Ω | Select-able multiplexer to OUT0OUT8 blocks, Optical clock, Optical clock/2 | Logic level or pulse with programmable timing |
| CM TRIG OUT | Common trigger, general purpose output | 2.5 V @ 50 Ω | OUT0 block, programmable pulse parameters | Logic level or pulse with programmable timing |
| SYNC IN | External synchronization input. Trigger or Configuration switch source | LVTTL 0.1 mA pull down to low level | Frequency \leq 100 MHz, PW \geq 10 ns | Positive pulse |
| GATE IN | Burst trigger or configuration switch control functions | LVTTL, 0.1 mA pull down to low level | Level or pulse with PW > 20 ns | Level or pulse |

A-SIDE BNC CONNECTORS

| Name | Direction | Logic levels | Impedance | Function |
|-------------|-----------|---|------------------|--|
| PRET OUT | Output | >1.5 V @ 50 Ω | 50 Ω | Precision trigger, configurable source |
| TRIG1 OUT | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | General trigger, configurable source |
| CM TRIG OUT | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | Master trigger, OUT0 signal |
| SYNC IN | Input | LVTTL, tolerates 5 V | 0.2 mA pull down | Trigger input |
| GATE IN | Input | LVTTL, tolerates 5 V | 0.2 mA pull down | Configuration switch and burst control input |





COAXIAL CONNECTORS, B-SIDE, MCX TYPE

| Name | Description | Amplitude | Pulse parameters | Shape |
|--------------|---|--------------|---|--|
| AN OUT | DAC output | 01 V | N/A | Two programmable analog levels |
| CM TRIG OUT | Common trigger, general purpose output | 2.5 V @ 50 Ω | OUT0 block | Logic level or pulse with programmable timing |
| CM TRIG OUT1 | Common trigger, general purpose output | 2.5 V @ 50 Ω | OUT0 block | Logic level or pulse with programmable timing |
| OUT2 | General purpose output | 2.5 V @ 50 Ω | OUT2 block, AND+OR+NOT logic with OUT1 | Logic level or pulse with programmable timing |
| OUT3 | General purpose output | 2.5 V @ 50 Ω | OUT3 block, AND+OR+NOT logic with OUT2 | Logic level or pulse with programmable timing |
| OUT4 | General purpose output | 2.5 V @ 50 Ω | OUT4 block, AND+OR+NOT logic with OUT3 | Logic level or pulse with programmable timing |
| OUT5 | General purpose output | 2.5 V @ 50 Ω | OUT5 block, AND+OR+NOT logic with OUT4 | Logic level or pulse with programmable timing |
| CLC IN | External clock input | >100 mV | PW >300ps, input frequency 10100 MHz | Sine, Meander to pulse train from photodiode |

B-SIDE MCX CONNECTORS

| Name | Direction | Logic levels | Impedance | Function |
|--------------|-----------|---|-----------|--------------------------------------|
| AN OUT | Output | 1 V @ 50 Ω max | 50 Ω | DAC analog output signal |
| CM TRIG OUT | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | Master trigger, OUT0 signal |
| CM TRIG OUT1 | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | Master trigger, OUT0 signal |
| OUT2 | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | General purpose trigger, OUT2 signal |
| OUT3 | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | General purpose trigger, OUT3 signal |
| OUT4 | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | General purpose trigger, OUT4 signal |
| OUT5 | Output | 2.5 V @ 50 Ω, 4.5 V @ 50 Ω jumper configurable | 50 Ω | General purpose trigger, OUT5 signal |
| CLC IN | Input | 0.5 V3.3 V pk-pk, sine or pulses | 50 Ω | Clock input |

DRAWINGS



Outline drawings of SY4000 OEM version



Outline drawings of SY4000 desktop version

